AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior versions of claims in the application.

LISTING OF THE CLAIMS:

Claims 1-10 (Cancelled).

Claim 11 (Original): A method of manufacturing a semiconductor device comprising steps of:

forming an interlayer insulating film on a surface of a substrate having an insulating surface, formed with semiconductor elements, and having a conductive member exposed in a partial area of the insulating surface;

forming a first antireflection film on the interlayer insulating film, the first antireflection film suppressing reflection in an absorption mode;

forming a second antireflection film on the first antireflection film, the second antireflection film suppressing reflection in a countervailing interference mode;

forming a cap film on the second antireflection film;

forming a first photosensitive resist film on the cap film;

exposing the first photosensitive resist film to light of a first wavelength, developing the exposed film to form an opening through the first photosensitive resist film, the opening corresponding to a via hole for connecting a wiring pattern to be formed on the interlayer insulating film to the conductive member;

etching the interlayer insulating film to form the via hole by using the first photosensitive resist film as a mask;

removing the first photosensitive resist film;

forming a second photosensitive resist film on the cap film;

exposing the second photosensitive resist film to light of the first wavelength, developing the exposed film to form an opening through the second photosensitive resist film, the opening corresponding to the wiring pattern to be formed on the interlayer insulating film;

etching the interlayer insulating film to form a wiring groove by using the second photosensitive resist film as a mask, the wiring groove reaching a midst of the interlayer insulating film in a thickness direction thereof;

removing the second photosensitive resist film;

deepening the via hole until the conductive member is exposed if the conductive member is not exposed on a bottom of the via hole; and

burying an inside of the via hole and the wiring groove with a conductive wiring material.

Claim 12 (Original): A method of manufacturing a semiconductor device according to claim 11, wherein an attenuation coefficient of the cap film at the first wavelength is smaller than an attenuation coefficient of the second antireflection film at the first wavelength.

Claim 13 (Original): A method of manufacturing a semiconductor device according to claim 11, wherein an attenuation coefficient of the cap film at the first wavelength is 0.

Claim 14 (Original): A method of manufacturing a semiconductor device according to claim 11, wherein an attenuation coefficient of the first antireflection film is 1 or higher at the first wavelength.

Claim 15 (Original): A method of manufacturing a semiconductor device according to claim 11, wherein an attenuation coefficient of the second antireflection film is 0.9 or lower at the first wavelength.

Claims 16-17 (Cancelled).